REMARKS

Claims 1-13, 20 and 21 are pending in the present application. Claims 1, 2, 4, 5, 7, 8, 11 and 13 have been amended, Claims 14-19 have been cancelled, and Claims 20 and 21 have been added, herewith. Reconsideration of the pending claims is respectfully requested.

Applicants would initially like to thank the Examiner for taking the time to conduct a telephonic interview on 06/29/2004. While no agreement was reached, Applicants representative discussed how the register control using thread control signals per the present invention was directed to pipelining, whereas the cited reference used thread control signals to controlled instruction buffers which are further upstream in the overall logic flow.

I. Claim Objection

The Examiner objected to Claims 14 and 17 due to a typographical error (a missing word of "or"). As such claims have been cancelled herewith without prejudice or disclaimer, this claim objection is now moot.

II. 35 U.S.C. § 112, Second Paragraph

The Examiner rejected Claims 1, 4, 7, 10, 13 and 17 under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter, which applicants regard as the invention. This rejection is respectfully traversed as to the claims as amended.

With respect to Claim 1, the Examiner states it is unclear whether the latches and registers select the thread, or rather the control signal selects the thread. Applicants have amended Claim 1 to clarify operation of the thread control signals.

With respect to Claim 4, the Examiner states that it is unclear what mode the processor was in prior to be returned to an interleaving mode. Applicants have amended Claim 4 to clarify this matter, by eliminating the terminology 'returning'.

Regarding Claim 7, the Examiner states the bus coupling is unclear. Applicants have amended Claim 7 to clarify that the bus coupling is with respect to the processor and memory unit.

PAGE 8/12 * RCVD AT 7/7/2004 4:29:16 PM [Eastern Daylight Time] * SVR:USPTO-EFXRF-1/2 * DNIS:8729306 * CSID:9723672008 * DURATION (mm-ss):03-20

Further regarding Claim 7, the Examiner states that there is insufficient antecedent basis for the multimedia multithreading processor (and that Claims 13 and 17 have similar problems). Applicants have amended Claims 7 and 13 accordingly (Claim 17 has been cancelled herewith, without prejudice or disclaimer).

Therefore the rejection of claims 1, 4, 7, 10, 13 and 17 under 35 U.S.C. § 112, second paragraph has been overcome.

III. 35 U.S.C. § 102, Anticipation

The Examiner rejected Claims 1-12 and 14-19 under 35 U.S.C. § 102(b) as being anticipated by Parady, U.S. Patent No. 5,933,627. This rejection is respectfully traversed as to the claims as amended.

With respect to Claim 1 (and similarly for Claim 7), such claim has been amended in accordance with the embodiment described at Specification page 9, lines 9-25 and now recites that the thread control signals are delayed from one another – and specifically a control signal for the hold latches is delayed from a control signal for the register file when switching between threads to thereby accommodate efficient thread switching when pipelining instructions for execution. As can be seen by FIG. 3 of the cited Parady reference, the thread control signals from thread switching logic block 112 are coupled to PA registers 110, register files 48 and 50, and thread instruction buffers 102, 104, 106 and 108. As described by Parady at Col. 3, lines 35-43, pipelining is provided within instruction unit 41 (such pipelines being shown at elements 32-46 in FIG. 1). However, it should be noted that the thread switch control signals are not coupled to instruction unit 41 or the pipelines contained therein. Instead, these control signals are coupled further upstream in the logic flow, and are coupled to instruction buffers 102-108 where they are used to enable a given thread instruction buffer such that that one of the thread instruction buffers provides instructions to dispatch unit 128 for dispatch to instruction units 41 (Col. 3, lines 38-42). In order to switch between threads, the dispatch unit begins dispatching instructions from another of the thread instruction buffers as enabled by the thread control signal from the thread switching logic 112. Because of this Parady architecture, where the thread control signals are used to selectively enable a thread instruction buffer to read and then dispatch an instruction well before any pipelining operation, there would

PAGE 9/12 * RCVD AT 7/7/2004 4:29:16 PM [Eastern Daylight Time] * SVR:USPTO-EFXRF-1/2 * DNIS:8729306 * CSID:9723672008 * DURATION (mm-ss):03-20

be no need to delay a thread switching control signal for certain logic blocks being controlled by such signal, with respect to other logic blocks being controlled by another thread switching control signal, to accommodate pipelining as claimed. Thus, in addition to not being anticipated by the cited reference, it is shown that there would not have been any motivation to modify Parady's teachings in accordance with the claimed invention, and hence amended Claim 1 (and similarly for Claim 7) is also shown to not be obvious in view of the cited reference.

Applicants traverse the rejection of Claims 2-6 and 8-12 for similar reasons to those given above regarding independent Claims 1 and 7, of which these Claims 2-6 and 8-12 depend upon.

With respect to Claims 14-19, Applicants have cancelled such claims herewith without prejudice or disclaimer.

Therefore, the rejection of Claims 1-12 and 14-19 under 35 U.S.C. § 102 has been overcome.

IV. 35 U.S.C. § 103, Obviousness

The Examiner rejected Claim 13 under 35 U.S.C. § 103 as being unpatentable over Parady, U.S. Patent No. 5,933,627 in view of Patterson et al., *Computer Organization & Design: The Hardware/Software Interface.* This rejection is respectfully traversed.

Applicants initially traverse the rejection of Claim 13 for similar reasons to those given above regarding Claim 7, of which Claim 13 depends upon.

Applicants further show that the Examiner is using improper hindsight analysis in rejecting Claim 13. It is error to reconstruct the patentee's claimed invention from the prior art by using the patentee's claims as a "blueprint". When prior art references require selective combination to render obvious a subsequent invention, there must be some reason for the combination other than the hindsight obtained from the invention itself. *Interconnect Planning Corp. v. Feil*, 774 F.2d 1132, 227 USPQ 543 (Fed. Cir. 1985). Further, as stated by the Federal Circuit, "virtually all [inventions] are combinations of old elements." *Environmental Designs, Ltd. v. Union Oil Co.*, 713 F.2d 693, 698, 218 USPQ 865, 870 (Fed. Cir. 1983); *see also Richdel, Inc. v. Sunspool Corp.*,

PAGE 10/12 * RCVD AT 7/7/2004 4:29:16 PM [Eastern Daylight Time] * SVR:USPTO-EFXRF-1/2 * DNIS:8729306 * CSID:9723672008 * DURATION (mm-ss):03-20

714 F.2d 1573, 1579-80, 219 USPQ 8, 12 (Fed. Cir. 1983) ("Most, if not all, inventions are combinations and mostly of old elements."). Therefore an examiner may often find every element of a claimed invention in the prior art. If identification of each claimed element in the prior art were sufficient to negate patentability, very few patents would ever issue. Furthermore, rejecting patents solely by finding prior art corollaries for the claimed elements would permit an examiner to use the claimed invention itself as a blueprint for piecing together elements in the prior art to defeat the patentability of the claimed invention. Such an approach would be "an illogical and inappropriate process by which to determine patentability." *Sensonics, Inc. v. Aerosonic Corp.*, 81 F.3d 1566, 1570, 38 USPQ2d 1551, 1554 (Fed. Cir. 1996). "[w]hen determining the patentability of a claimed invention which combines two known elements, 'the question is whether there is something in the prior art as a whole to suggest the desirability, and thus the obviousness, of making the combination.'" *See In re Beattie*, 974 F.2d 1309, 1311-12, 24 USPQ2d 1040, 1042 (Fed. Cir. 1992) (quoting *Lindemann Maschinenfabrik GmbH v. American Hoist & Derrick Co.*, 730 F.2d 1452, 1462, 221 USPQ 481, 488 (Fed. Cir. 1984)). There is simply nothing in the cited art to suggest combining two mixed-mode multithreading processors together. The only suggestion comes from Applicants' own patent specification, which is improper hindsight analysis.

As further basis for the rejection of Claim 13, the Examiner states that inclusion of a second processor provides no new or unexpected result over the prior art of record. Applicants show that, to the contrary, the advantages of using mixed-mode multithreading in a multi-processing system are described in the present Specification at page 1, lines 16-20 and page 7, lines 5-28. The new and unexpected result that is provided by Claim 13 is mixed-mode multi-threading in a multi-processing system, whereby each processor provides mixed-mode multithreading capabilities to further enhance overall system performance and throughput.

Therefore, the rejection of Claim 13 under 35 U.S.C. § 103 has been overcome.

V. Newly added Claims

Applicants have added Claims 20 and 21 herewith. Examination of such claims is respectfully requested.

PAGE 11/12 * RCVD AT 7/7/2004 4:29:16 PM [Eastern Daylight Time] * SVR:USPTO-EFXRF-1/2 * DNIS:8729306 * CSID:9723672008 * DURATION (mm-ss):03-20

VI. Conclusion

It is respectfully urged that the subject application is patentable over the cited references and is now in condition for allowance. The Examiner is invited to call the undersigned at the below-listed telephone number if in the opinion of the Examiner such a telephone conference would expedite or aid the prosecution and examination of this application.

DATE: 7/7/04

Respectfully submitted,

Duke W. Yee
Reg. No. 34,285
Wayne P. Bailey
Reg. No. 34,289
Yee & Associates, P.C.
P.O. Box 802333
Dallas, TX 75380
(972) 367-2001
Attorneys for Applicants

PAGE 12/12 * RCVD AT 7/7/2004 4:29:16 PM [Eastern Daylight Time] * SVR:USPTO-EFXRF-1/2 * DNIS:8729306 * CSID:9723672008 * DURATION (mm-ss):03-20